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For: **MODIFICATION OF COLUMN FIXED PATTERN NOISE IN SOLID STATE IMAGE SENSORS**

TRANSMITTAL OF CERTIFIED PRIORITY DOCUMENT

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Respectfully submitted,

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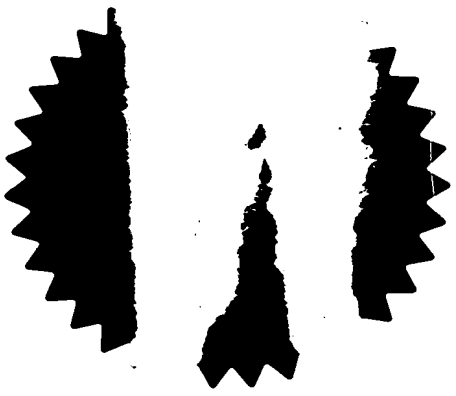

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By virtue of a direction given under Section 30 of the Patents Act 1977, the application is proceeding in the name of

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SECTION 30(1977 ACT) APPLICATION FILED

Patents ADP number *(if you know it)*

If the applicant is a corporate body, give the country/state of its incorporation

United Kingdom

4. Title of the invention

"Modification of Column Fixed Pattern Column Noise in Solid State Image Sensors"

5. Name of your agent *(if you have one)*

Murgitroyd & Company

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1198013

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"Modification of Column Fixed Pattern Column Noise in Solid State Image Sensors"

The present invention relates to techniques for ameliorating the effects of column fixed pattern noise in solid state image sensors of the type comprising a matrix of photoelectric conversion elements ("pixels", typically comprising photodiodes, for example, in an image sensor implemented using CMOS technology). The techniques of the invention result in column fixed pattern noise being modulated (or dithered) in a manner which makes the noise less apparent to the eye and which facilitates subsequent cancellation of the noise.

In an image sensor of this general type, the pixels are arranged in rows and columns and each pixel has a read switch which connects the pixel to a vertical line. Horizontal control lines activate the read switches of a row of pixels. These lines are pulsed in sequence in order to read the light dependent pixel voltages onto the vertical lines. A vertical shift register or decoder is commonly used to generate the read pulse

sequence. The voltages on the vertical column lines then pass through a set of elements, one per column, which process the pixel output signals. Typical operations performed by the column elements include storage, amplification, buffering and analog-digital (AD) conversion.

The column elements add noise in the form of offset voltages to the pixel voltages. The offsets added by each column element vary randomly from column element to column element, substantially the same offset being applied to each pixel in a given column. This results in vertical shading of the output image, known as "column fixed pattern noise" ("column FPN"). The main sources of the offsets are mismatches in the charge injection of the sampling switches and amplifier offsets.

It is known to remove column FPN by calibrating the image sensor to compensate for the offsets which give rise to column FPN. The sensor is calibrated by applying a known voltage to the inputs of each column element. The resulting column outputs allow the offset for each column to be measured and stored. The measured offsets can subsequently be subtracted from the pixel outputs by analog or digital means. The calibration operation can be performed once per line or once per field. If it is performed once per line, it reduces the time available for pixel conversion. If it is performed once per field, then care must be taken that random thermal noise does not affect the results and that calibration is not influenced by effects not

present during normal pixel readout. Such techniques necessarily increase the cost of the sensors.

Solid state image sensors are commonly combined with an analog-digital-conversion ("ADC") function. Two ADC architectures are in common use: per-chip ADC and per-column ADC. In the former, a single high-speed ADC is used to convert all column pixel outputs downstream of the column elements. In the latter, a low speed ADC is incorporated into each column, suitably as part of the column element, so that the analog values of each pixel output voltage of each row are converted in parallel.

Fig. 1 illustrates a conventional per-chip ADC solid state image sensor architecture, comprising a matrix of pixels 10 (a 3x3 matrix is shown for the purposes of illustration, the actual matrix would normally be much larger), associated read switches 12, vertical shift register (decoder) 14, column element circuits 16 and horizontal shift register (decoder) 18. An analog readout bus 20 is connected to the single ADC 22. The ADC may be external ("off-chip"), in which case the analog pixel signals must be driven off-chip, which often requires extra buffering. Alternatively, the ADC may be integrated on-chip with the rest of the sensor, improving speed and power consumption and reducing overall cost. The column elements 16 typically comprise storage capacitors, buffer amplifiers and access switches driven by the horizontal decoder 18. The storage elements hold the pixel voltages ready for conversion by the ADC 22. Buffer amplifiers are required to drive the readout bus 20 and ADC input

capacitance. Charge injection of the sampling switches and amplifier offset both contribute to column FPN.

Fig. 2 illustrates a conventional per-column ADC solid state image sensor architecture, again comprising a matrix of pixels 10, read switches 12, vertical decoder 14, column element circuits 24, incorporating per-column ADC, and horizontal decoder 18. A digital readout bus 26 provides the sensor output. The column elements 24 include ADC elements, typically comprising sampling capacitors, reference voltage input (REF), comparator and digital storage elements. The storage elements hold the pixel voltages for comparison with the reference by the comparator. Charge injection of the sampling switches and amplifier offset again contribute to column FPN.

It is an object of the present invention to provide improved techniques for cancelling column FPN in solid state image sensors which do not add significantly to the cost of the sensor and which are suitable for implementation in CMOS-type image sensors.

In accordance with a first aspect of the invention, there is provided a method of operating a solid state image sensor of the type comprising an array of photosensitive pixels arranged in rows and columns and in which pixel data signals are read out from said pixels via column circuits which introduce column fixed pattern noise to said signals, comprising the steps of selectively inverting said signals input to said column

circuits and reversing said inversion following output from said column circuits.

In certain embodiments, said selective inversion is applied to alternate rows of said pixel data. In other embodiments, said selective inversion is applied to alternate groups of rows of said pixel data, particularly alternate pairs of rows of said pixel data.

In certain embodiments, said selective inversion is applied differently to different frames of said pixel data. For example, a first selective inversion scheme is applied to alternate frames and a second selective inversion scheme opposite to said first selective inversion scheme is applied to intervening frames.

In certain embodiments, the method preferably further includes the step of selectively switching outputs from adjacent columns between adjacent column output channels prior to said selective inversion of said signals input to said column circuits.

In accordance with a second aspect of the invention, there is provided a solid state image sensor of the type comprising an array of photosensitive pixels arranged in rows and columns and in which pixel data signals are read out from said pixels via column circuits which introduce column fixed pattern noise to said signals, further including means for selectively inverting said signals input to said column circuits

and means for reversing said inversion following output from said column circuits.

In certain embodiments, said means for selectively inverting said signals includes a first chopping circuit included in each column at the input to each column circuit.

Where the sensor is of the active pixel type in which pixel signal voltages and reset voltages are input to said column circuits, said means for selectively inverting said signals input to said column circuits may comprise switch means and control means associated therewith for sampling said pixel signal voltages and reset voltages.

Preferably, said means for reversing said inversion comprises at least one output chopper circuit. In certain embodiments, each column of said array includes an output chopper circuit.

In certain embodiments, each column circuit includes analog-to-digital conversion means and said output chopper circuit comprises digital inversion means.

Preferably, said selective inversion and re-inversion is controlled by a common chopping signal.

In certain embodiments, the sensor further includes means for selectively switching outputs from adjacent columns between adjacent column output channels prior

to said means for selectively inverting said signals input to said column circuits.

In accordance with a third aspect of the invention, there is provided an imaging system incorporating a solid state image sensor in accordance with the second aspect of the invention.

In accordance with a fourth aspect of the invention, there is provided a camera incorporating a solid state image sensor in accordance with the second aspect of the invention.

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Fig. 1 illustrates a conventional solid state image sensor having a per-chip ADC architecture;

Fig. 2 illustrates a conventional solid state image sensor having a per-column ADC architecture;

Fig. 3 illustrates an embodiment of a solid state image sensor having a per-chip ADC architecture in accordance with the present invention;

Fig. 4 illustrates an embodiment of a solid state image sensor having a per-column ADC architecture in accordance with the present invention;

Fig. 5 illustrates a chopper circuit for use in accordance with the present invention;

Fig. 6 illustrates an embodiment of a circuit for implementing column FPN reduction in accordance with the present invention;

Fig. 7 illustrates a further embodiment of a circuit for implementing column FPN reduction in accordance with the present invention; and

Fig. 8 illustrates an embodiment of a combined column circuit and multiplexer for implementing column FPN reduction in accordance with the present invention.

Referring now to the drawings, Fig. 3 shows an embodiment of a solid state image sensor with a per-chip ADC architecture, similar to that of Fig. 1, but modified to implement a column FPN reduction technique in accordance with the present invention. As in Fig. 1, the sensor comprises a matrix of pixels 100, associated read switches 102, vertical shift register (decoder) 104, column element circuits 106, horizontal shift register (decoder) 108, analog readout bus 110 and ADC 112. In addition, each column includes a first chopper circuit 114 upstream of the respective column element 106, and the readout bus 110 includes a second chopper circuit 116 downstream of the column elements 106 and prior to the ADC 112. The operation of the chopper circuits 114 and 116 is controlled by a common CHOP signal circuit 118.

Fig. 4 shows an embodiment of a solid state image sensor with a per-column ADC architecture, similar to that of Fig. 2, but again modified to implement a column FPN reduction technique in accordance with the present invention. As in Fig. 3, the sensor comprises a matrix of pixels 200, associated read switches 202, vertical shift register (decoder) 204, column element circuits 206 incorporating ADC means, horizontal shift register (decoder) 208 and digital readout bus 210. In addition, each column includes a first chopper circuit 214 upstream of the respective column element 206, and a second chopper element 216 downstream of the respective column element 206. The operation of the chopper circuits 114 and 116 is controlled by a common CHOP signal circuit 218.

The function and operation of the chopper circuits/elements 114, 116, 214, 216 etc. of the present invention will now be described in more detail.

Referring firstly to Fig. 7, there is shown an implementation of the present invention as applied to each column of a prior art sensor such as that of Fig. 2, (i.e. having a per-column ADC architecture). Fig. 7 shows one pixel 300 of a plurality pixels which together make up one column of a sensor array, and a column circuit 302. The pixel 300 in this case is an active three-transistor type, comprising a photodiode 304, a reset switch transistor 308, a read switch transistor 310 and an amplifying transistor 312, as is well know in the art. As previously noted, the decoder (vertical and horizontal shift registers 14,16 of Fig.

2) allows selective reset of a row of pixels from a reference voltage (VRT) and subsequent read of the light-dependent pixel output voltages.

In the horizontal direction each of the column circuits includes an ADC element 306 which together convert a row of pixel output voltages to digital form. Each individual column circuit 302 includes a pair of switches 314, 316 to control sampling of the pixel signal voltage (Vsig) and the reset voltage (Vbck) respectively onto a pair of storage capacitors 318 (Csig) and 320 (Cbck). The switches 314, 316 are controlled by control signals (CDSSIG and CDSBCK) which are activated once per row to store the output voltages of the row of pixels currently being read. The sampling capacitors 318, 320 present their stored voltages to the ADC element 306 whose output controls the access switches of a register of memory elements 322. An addressable decoder allows selective read of the memory elements 322.

Analog to digital conversion is achieved by comparison of the differential input voltage to the ADC 306 (Vsig - Vbck) of each column against a global ramp voltage (Vrmp) generated by a ramp generator 324, which is swept over a suitable range. When an individual ADC element 306 detects that the ramp voltage is greater than the differential input voltage (Vsig - Vbck) the ADC output changes from a logic low state to logic high. During the ramp voltage sweep a digital word GCC is incremented by counter 325 and made accessible to the memory element 322 in each column. On a low to

high transition of a column ADC element 306, the current value of this count is stored by the column memory element 322. The stored count value is then a digital representation of the magnitude of the differential input voltage (Vsig - Vbck). Once the Vrmp and GCC sweep is completed, the row of digital codes in the memory elements 322 is read out by addressing the horizontal decoder (18 in Fig. 2).

The column circuitry and functionality as described thus far in relation to Fig. 7 is conventional, as would be employed in a sensor of the type shown in Fig. 2. Column FPN is introduced by mismatches in the column ADC and sampling elements. It has the effect of adding an offset voltage Vfpn to each column differential voltage (Vsig - Vbck + Vfpn). The voltages Vfpn are randomly distributed across the array and their contributions appear as shaded vertical lines in the output image. The main sources of offset are mismatches in the charge injection of the sampling switches and amplifier offsets.

In the embodiment of Fig. 7, modulation of column FPN is accomplished as follows. The phases of the control signals CDSSIG and CDSBCK for the switches 314 and 316 are interchanged after every pair of lines. On odd pair rows operation is as normal; i.e. the pixel signal voltage Vsig is stored on the first storage capacitor 318 and the reset voltage Vbck is stored on the second storage capacitor 320. On even pair rows this phase interchange has the effect of storing the pixel reset voltage Vbck on the first storage capacitor 318 and the

pixel signal voltage Vsig on the second storage capacitor 320. That is, the differential voltage presented to the ADC element 306 is inverted whilst the offsets remain in the same sense: (Vbck - Vsig +Vfpn).

In addition, a first chopper circuit or multiplexer 326 at the output of the ramp generator 324 inverts the sense of reference ramp voltage Vrmp on even pair rows. Since both the signal and reference are inverted at the ADC element input, the ADC output is also inverted and now produces a one-to-zero transition when the ramp voltage Vrmp exceeds the pixel differential voltage. The ADC output is inverted by a second chopper circuit 328 after every even row pair to maintain consistent operation of the memory element 322 and GCC. The AD conversion thus provides a digital representation of the value (Vsig - Vbck + Vfpn) on odd pair rows and (Vbck - Vsig + Vfpn) on even pair rows. This has the effect of modulating the column FPN to a high frequency which can be corrected during subsequent colour reconstruction of the image sensor output signal. The inverting or "chopping" action is performed on a row pair basis in order to avoid corrupting colour information from the Bayer pattern colour filter array of the sensor.

The various inversion operations are controlled by a CHOP signal. Fig. 7 shows a timing diagram 330 illustrating the CHOP signal and the corresponding phase inversion of the control signals CDSSIG and CDSBCK. The same CHOP signal also controls the

operation of the first and second chopper signals as described above.

The embodiment of Fig. 7 also makes it possible to vary the chopping action on a frame-by-frame basis; e.g. to chop on even row pairs on even frames and on odd row pairs on odd frames. In this manner, the fixed pattern noise offset on any given pixel changes sign from frame to frame. In a 30 frame-per-second (fps) sensor, all pixels would thus exhibit a 15fps cyclic FPN inversion. Averaging in the retina of the viewer's eye will then help to attenuate the apparent FPN.

In a monochrome camera, it is possible to chop on a row-by-row basis so as to obtain a high frequency noise pattern which is less noticeable to the eye. A noise pattern of this type may be acceptable in high-resolution monochrome images without the need for additional correction, representing a saving in hardware for single-chip video cameras.

The present invention is applicable to all solid-state image sensors having a matrix of photosensitive elements (pixels), typically photodiodes, and is particularly applicable to such sensors implemented using CMOS technology.

The invention may be implemented in other ways, besides that described above with reference to Fig. 7. In general terms, the invention requires a chopping action to be applied to the inputs and outputs of the column circuits of conventional image sensors such as those of

Figs. 1 and 2, as illustrated in Figs. 3 and 4. The "input" choppers (114 and 214 in Figs. 3 and 4) have the function of inverting the polarity (or logic state) of the input signal whilst the "output" choppers (116, 216 in Figs. 3 and 4) invert the polarity (or logic state) of the output signal, both under the control of the CHOP timing signal. In these examples, when CHOP is high no inversion is performed and when CHOP is low the signal polarity is inverted. If the function of the column circuits (106 and 206 in Figs. 2 and 3) is considered to be linear (gain and/or delay) with additive offset noise, then the periodic inversion only affects the offset. That is, the inversion of the input signal by the input choppers is reversed by the output choppers, whilst the offset noise, which arises within the column circuits, is inverted once by the output choppers.

The function of the conventional column circuits can be represented generically as:

$$V_o(t) = V_i(t)gz^{-1} + V_{off}$$

where $V_o(t)$ is the column output signal, $V_i(t)$ is the column input signal (equivalent to Vsig-Vbck above), g is a gain, z^{-1} is a delay and V_{off} is an offset (equivalent to Vfpn above). If the input and output are multiplied by the function $s(t) = 1$ when CHOP = 1 and $s(t) = 0$ when CHOP = 0, then:

$$V_o(t) = V_i(t)gz^{-1}s(t)s(t) + V_{off}s(t)$$

which is equivalent to:

$$V_o(t) = V_i(t)gz^{-1} + V_{off}s(t)$$

since $s(t)*s(t) = 1$. This demonstrates that the effect of chopping is to invert only the offset term whilst the signal and the transfer function of the column circuit remain unchanged.

As discussed above, for Bayer pattern colour sensors the CHOP signal should remain high on even pair lines and should remain low on odd pair lines. This is to preserve offsets on Bayer colour cells which occur on a two-pixel repetition pattern in the horizontal and vertical directions. The chopped image can pass through colour processing without the noise information affecting colour reconstruction. The chopped offset noise component can be removed at a later stage by techniques such as spatial low-pass filtering etc.

As noted above, further improvements can be gained by varying the chopping action on a frame-by-frame basis. For example, by setting CHOP high on even row pairs and low on odd row pairs for even frames, and low for even row pairs/high for odd row pairs on odd frames, the offset noise component for any given pixel changes polarity from frame to frame. In a high frame-rate application, an averaging between successive frames will take place in the retina of the viewer's eye which will attenuate the apparent FPN noise amplitude which, in certain cases, may obviate the need for further FPN cancellation steps.

As also noted above, for monochrome image sensors, the CHOP signal should be set high on even lines and low on odd lines. The resulting noise pattern can be corrected in a similar way as for Bayer type colour sensors. However, the noise pattern has a higher spatial frequency since it is based on a single row cycle rather than a two-row cycle. The noise pattern is thus less noticeable to the eye and further FPN correction may not be necessary.

An advantage of the invention is that the offset noise information is modulated to a high spatial frequency where it is no longer correlated with the image. The offset information is therefore present in the image data in a form in which it can be selectively removed without degrading image quality. Prior art techniques of column FPN noise cancellation require special calibration cycles to be performed which slow down sensor operation. A further disadvantage of prior art techniques is that other noise sources may be present during calibration, which are not present during image read-out. These can cause new noise artefacts to be introduced by the compensation procedure.

The present invention requires a small amount of additional hardware per column in the form of the chopper circuits 114, 116 etc. at the inputs and outputs of the conventional column circuits 106 etc. However, the chopper circuits may be very simple. One example for differential signals (Vp - Vn) is illustrated in Fig. 5, comprising a set of four

switches controlled by the CHOP signal as shown to provide chopped output signals Vop and Von. The differential output is (Vp - Vn) when CHOP is high and (Vn - Vp) when CHOP is low.

For active pixel sensors, Vp and Vn represent the pixel signal voltage Vsig and reset voltage Vbck as described above. These signals are stored on two sampling capacitors at two different sampling instants to allow resetting of the pixel. They are later subtracted to remove low frequency pixel noise using a technique called correlated double sampling (CDS). In this case, as described in relation to Fig. 7, no additional chopping switches are needed at the input to the conventional column circuit, since the necessary signal inversion may be achieved by reversing the phasing of the control signals CDSSIG and CDSBCK which control the sampling switches 314 and 316. By removing the need for additional switches, a possible source of charge injection mismatch is avoided. Fig. 6 shows a generalised embodiment of the implementation illustrated in Fig. 7, where like components are designated by like reference numerals. In this case, the specific column/ADC/chopper architecture of Fig. 7 is replaced by a generic conventional column circuit 332 and an output chopper circuit 334 such as that of Fig. 5. In the case where per-chip ADC is used, the column output chopper circuits may be removed and replaced by a single output chopper circuit (116 in Fig. 3) at the input to the ADC (112 in Fig. 3).

For sensors having a digital column output, such as in the example of Fig. 4, where the column circuit 206 performs the ADC function, chopping of the outputs from the column circuits 206 must operate on logic states. In this case, the output chopper means 216 may be realised by a two-input exclusive-OR function, with one of the inputs connected to the logic output and the other connected to CHOP.

Fig. 8 shows a further embodiment of the invention applied to a Bayer type sensor. As is well known in the art, a Bayer pattern colour sensor array comprises a repeating pattern consisting two pixels 402, 404 of a first colour (normally green) one pixel 406 of a second colour (normally blue) and one pixel 408 of a third colour (normally red) across two rows and two columns. Each column includes a conventional column circuit 410 and signals are read out from the sensor by an address decoder 412. In this embodiment, each column includes a first chopper circuit 414 at the input to the column circuit 410 and a second chopper circuit 416 at the output from the column circuit, as before. In this case, a further multiplexer/chopper 418 is included for each pair of adjacent columns of the Bayer pattern, between the pixel array column outputs and the first choppers 414, and inter-connecting the adjacent columns, so as to switch the adjacent column outputs in accordance with the value of the CHOP signal.

In this way, successive green channel pixel values from the adjacent columns pass through the same column readout circuit 410 and have exactly opposite polarity

offset components. Shuffled colour readout techniques can be applied as well as aiding computation during colour reconstruction. This embodiment is implemented by adding the further chopper 418, crossing the adjacent columns, to the previously described chopped column circuits. Shuffled readout can then be applied to read out all odd then all even columns by addressing the column decoder 412 appropriately. This ensures that all green pixel data from each pair of columns passes through the same column circuitry and is grouped in time.

It will be understood that the present invention modifies column FPN noise components in output image data in such a manner that, in certain applications, the column FPN noise is "disguised" to such an extent that further FPN cancellation is unnecessary, and also simplifies the subsequent cancellation of column FPN where this is required.

Image sensors embodying the present invention may be incorporated in a variety of types of imaging systems and cameras.

Improvements and modifications may be incorporated without departing from the scope of the invention.

Claims

1. A method of operating a solid state image sensor of the type comprising an array of photosensitive pixels arranged in rows and columns and in which pixel data signals are read out from said pixels via column circuits which introduce column fixed pattern noise to said signals, comprising the steps of selectively inverting said signals input to said column circuits and reversing said inversion following output from said column circuits.

2. A method as claimed in Claim 1, wherein said selective inversion is applied to alternate rows of said pixel data.

3. A method as claimed in Claim 1, wherein said selective inversion is applied to alternate groups of rows of said pixel data.

4. A method as claimed in Claim 3, wherein said selective inversion is applied to alternate pairs of rows of said pixel data.

5. A method as claimed in any preceding Claim, wherein said selective inversion is applied differently to different frames of said pixel data.

6. A method as claimed in Claim 5, wherein a first selective inversion scheme is applied to alternate frames and a second selective inversion scheme opposite

to said first selective inversion scheme is applied to intervening frames.

7. A method as claimed in any preceding Claim, further including the step of selectively switching outputs from adjacent columns between adjacent column output channels prior to said selective inversion of said signals input to said column circuits.

8. A solid state image sensor of the type comprising an array of photosensitive pixels arranged in rows and columns and in which pixel data signals are read out from said pixels via column circuits which introduce column fixed pattern noise to said signals, further including means for selectively inverting said signals input to said column circuits and means for reversing said inversion following output from said column circuits.

9. A solid state image sensor as claimed in Claim 8, wherein said means for selectively inverting said signals includes a first chopping circuit included in each column at the input to each column circuit.

10. A solid state image sensor as claimed in Claim 8, wherein said sensor is of the active pixel type in which pixel signal voltages and reset voltages are input to said column circuits and wherein said means for selectively inverting said signals input to said column circuits comprise switch means and control means associated therewith for sampling said pixel signal voltages and reset voltages.

11. A solid state image sensor as claimed in any one of Claims 8 to 10, wherein said means for reversing said inversion comprises at least one output chopper circuit.

12. A solid state image sensor as claimed in Claim 11, wherein each column of said array includes an output chopper circuit.

13. A solid state image sensor as claimed in Claim 12, wherein each column circuit includes analog-to-digital conversion means and wherein said output chopper circuit comprises digital inversion means.

14. A solid state image sensor as claimed in any one of Claims 8 to 13, wherein said selective inversion and re-inversion is controlled by a common chopping signal.

15. A solid state image sensor as claimed in any one of Claims 8 to 13, further including means for selectively switching outputs from adjacent columns between adjacent column output channels prior to said means for selectively inverting said signals input to said column circuits.

16. An imaging system incorporating a solid state image sensor as claimed in any one of Claims 8 to 15.

17. A camera incorporating a solid state image sensor as claimed in any one of Claims 8 to 15.

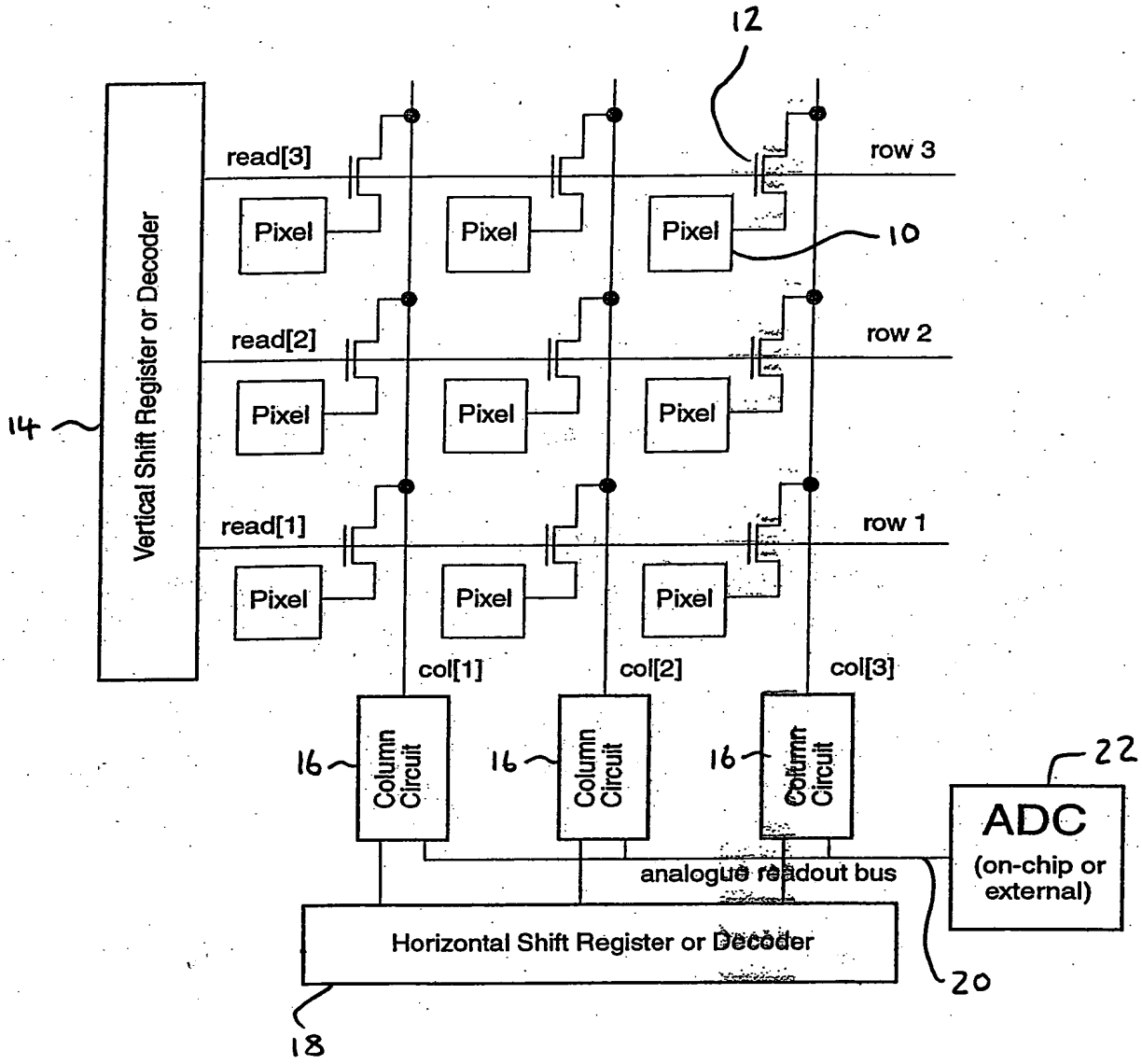

FIG. 1 (PRIOR ART)

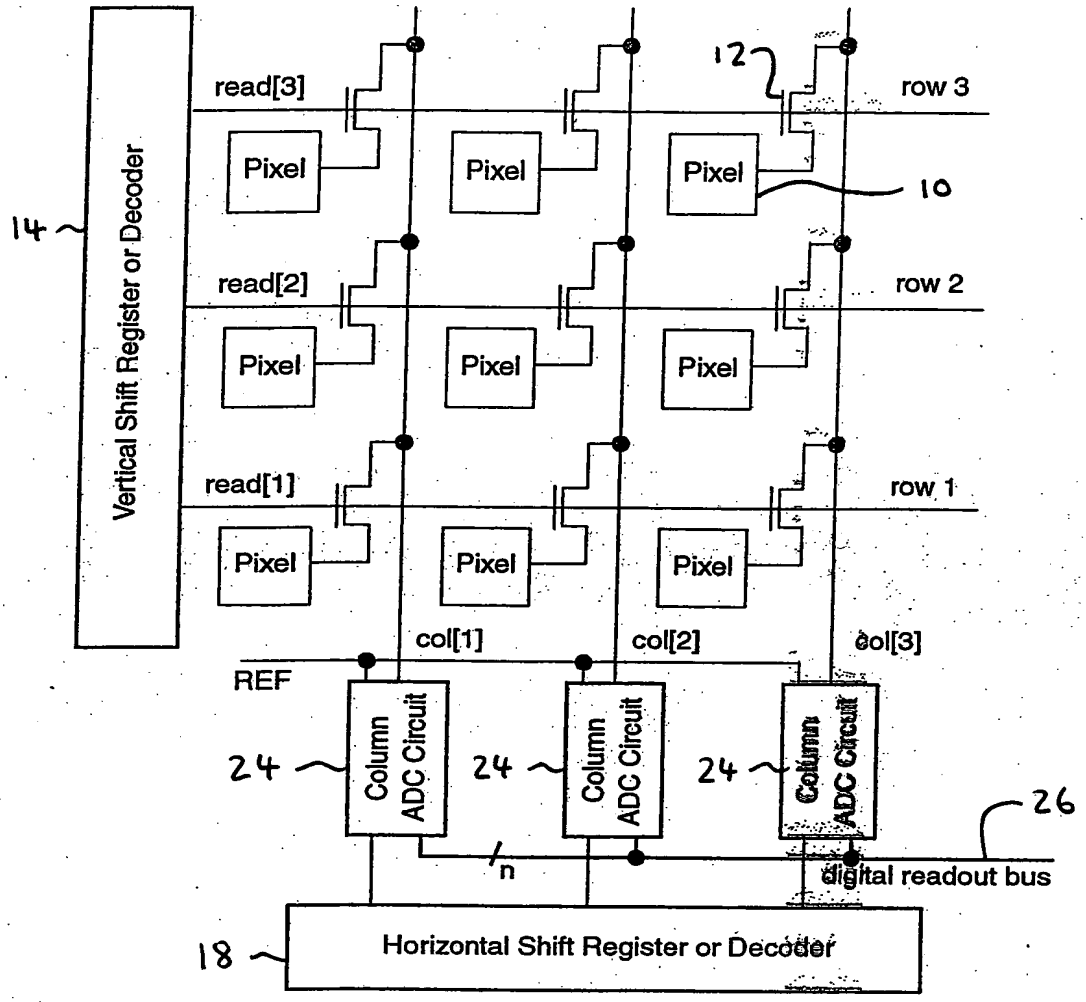

FIG. 2 (PRIOR ART)

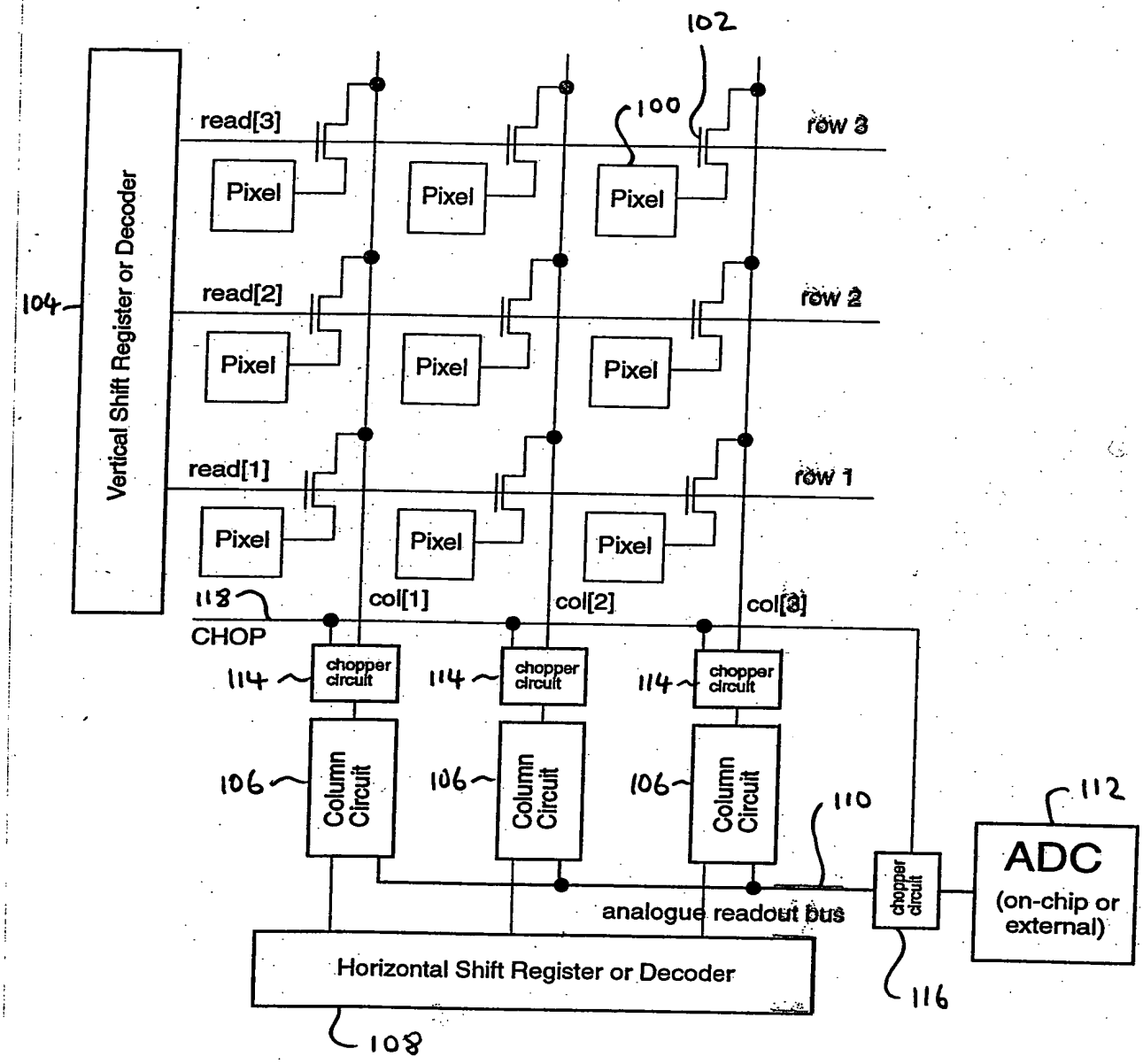
102
100
Vertical Shift Register or Decoder
104
read[3]
row 3
Pixel
Pixel
Pixel
read[2]
row 2
Pixel
Pixel
Pixel
read[1]
row 1
Pixel
Pixel
Pixel
118
CHOP
col[1]
col[2]
col[3]
chopper circuit
114
chopper circuit
114
chopper circuit
114
106
Column Circuit
106
Column Circuit
106
Column Circuit
110
chopper circuit
112
ADC
(on-chip or external)
analogue readout bus
Horizontal Shift Register or Decoder
116
108

Fig. 3

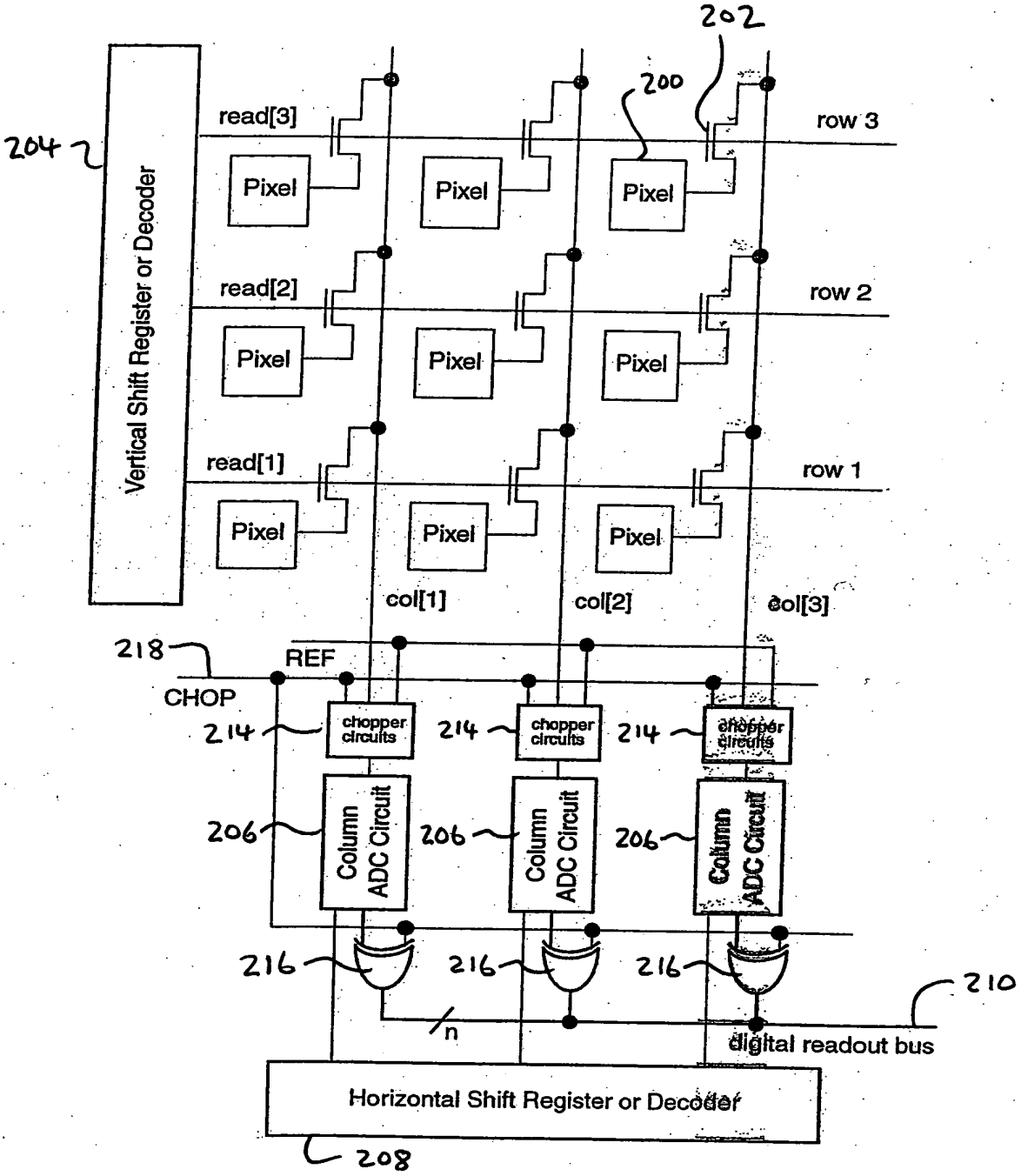
202
200
204
Vertical Shift Register or Decoder
read[3]
row 3
Pixel
Pixel
Pixel
read[2]
row 2
Pixel
Pixel
Pixel
read[1]
row 1
Pixel
Pixel
Pixel
col[1]
col[2]
col[3]
218
REF
CHOP
214
chopper circuits
214
chopper circuits
214
chopper circuits
206
Column ADC Circuit
206
Column ADC Circuit
206
Column ADC Circuit
216
216
216
210
n
digital readout bus
Horizontal Shift Register or Decoder
208

Fig. 4

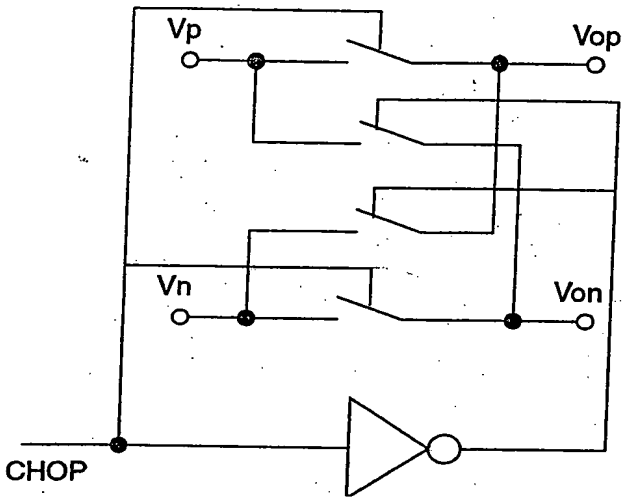
Vp
Vop
Vn
Von
CHOP

Fig. 5

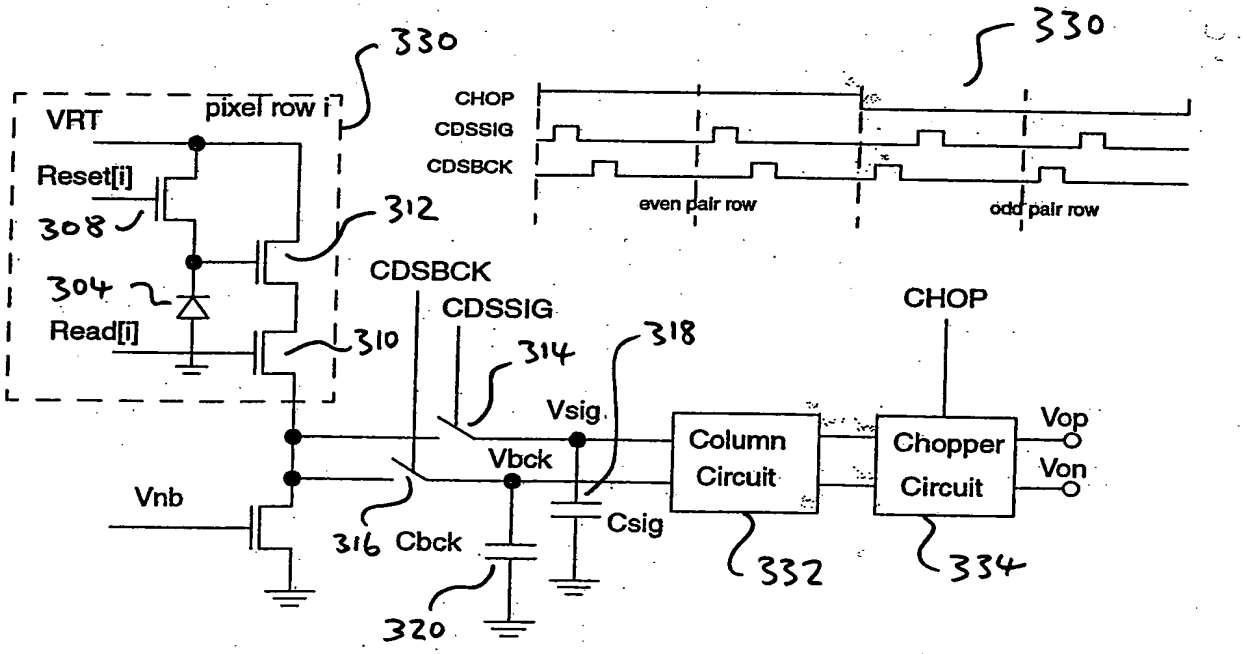
330
330
VRT
pixel row i
Reset[i]
308
304
Read[i]
312
310
CDSBCK
CDSSIG
314
318
316
Cbck
320
Vsig
Vbck
Vnb
Csig
Column Circuit
332
Chopper Circuit
334
CHOP
Vop
Von
CHOP
CDSSIG
CDSBCK
even pair row
odd pair row

Fig. 6

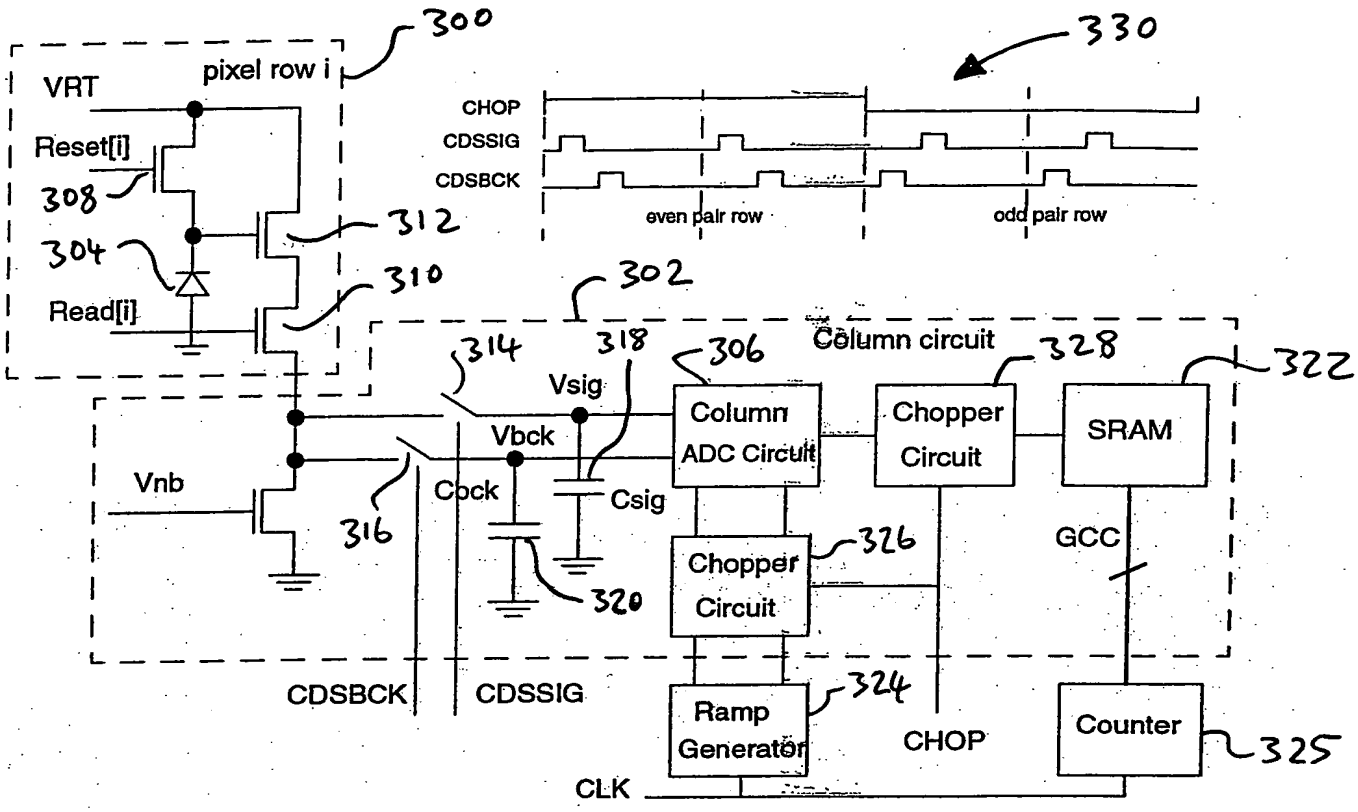
300
330
VRT
pixel row i
Reset[i]
308
304
312
310
Read[i]
CHOP
CDSSIG
CDSBCK
even pair row
odd pair row
302
314
318
306
Column circuit
328
322
Vsig
Vbck
Vnb
Cock
Csig
316
320
Column ADC Circuit
Chopper Circuit
SRAM
Chopper Circuit
326
GCC
CDSBCK
CDSSIG
Ramp Generator
324
CHOP
Counter
325
CLK

FIG. 7

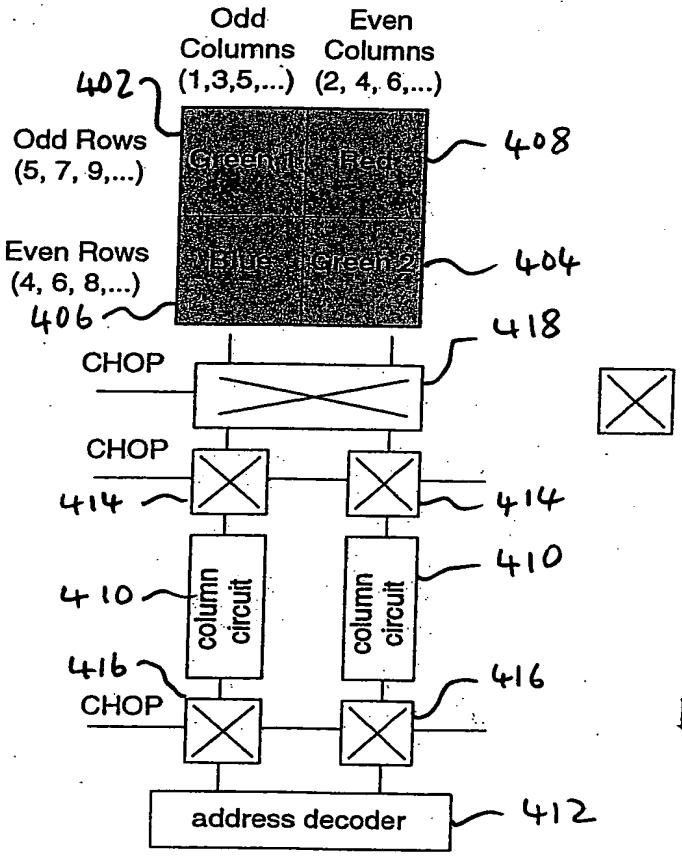
Odd Columns (1,3,5,...)
Even Columns (2, 4, 6,...)
402
Odd Rows (5, 7, 9,...)
Green 1
Red
408
Even Rows (4, 6, 8,...)
Blue
Green 2
404
406
418
CHOP
CHOP
414
414
410
column circuit
column circuit
410
416
CHOP
416
address decoder
412

FIG. 8